PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-159646

(43)Date of publication of application : 12.06.2001

(51)Int.Cl. G01R 21/08

(21)Application number : 11-344278

(22)Date of filing : 03.12.1999

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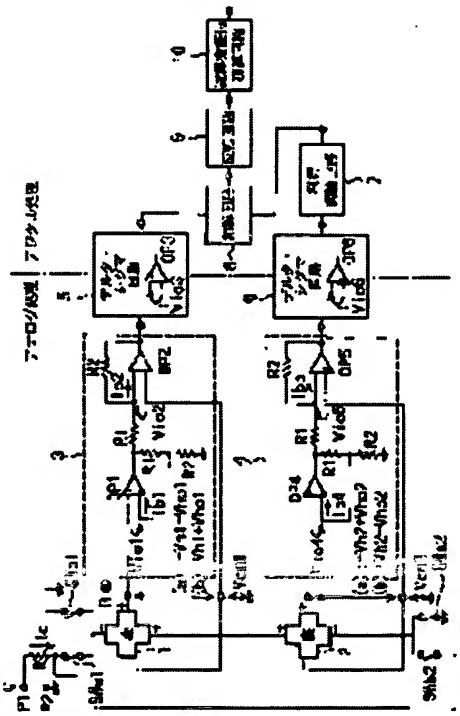
(54) WATTHOUR METER USING HALL ELEMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To accurately eliminate the unbalanced voltage of a Hall element causing an error, and the offset voltage of a differential amplification means.

SOLUTION: In the watthour meter, a Hall element outputs a Hall voltage corresponding to the product of measurement voltage and current, switching means Swa1 to Swb2 invert the positive and negative polarities of the Hall voltage at each specific period, differential amplification means 3 and 4 carry out differential amplification, an invert means 9 inverts the polarity of differential amplification output to a state where polarity invert is returned by the switching means again, and an integration means 10 performs integral calculus. Hall elements 1 and 2 for outputting an unbalanced voltage with the polarity being different from that of the Hall voltage with the same polarity are used, adjustment is made by an unbalanced voltage adjustment means 7 so that the unbalanced voltage of the two Hall elements becomes equal, and each differential amplification output of the two Hall elements is added by an addition means 8 before the integral calculus is made by the integral means 10.



LEGAL STATUS

[Date of request for examination] 23.01.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3462133
[Date of registration]	15.08.2003
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to amelioration of the watthour meter which measures electric energy using a hall device.
[0002]
[Description of the Prior Art] The basic configuration of the watthour meter using the hall device used conventionally is shown in drawing 3 . As for a hall device and 102, 101 is [a differential amplifying circuit and 103] integrating circuits. The volt input terminal P1 and P2 Hole current Ic which inputs the measurement electrical potential difference V and is equivalent to the measurement electrical potential difference V When the field B which is equivalent to a sink and the measurement current I through Resistance R is given, from a hall device 101, it is Hall voltage Vh =KxBxIc. It is outputted. Product sensitivity K is a constant which a hall device has. However, an unnecessary common mode voltage Vcm and offset voltage Vho are contained in power measurement from a hall device 101 at an output. A common mode voltage Vcm is an electrical potential difference contained in the output of both output terminal V+ of a hall device 101, and V-, and the value is the hole current Ic. It multiplies by the one half of the input resistance Rin of a hall device 101. Offset voltage Vho is Hall voltage Vh. It is the electrical potential difference similarly generated between output terminal V+ and V-, and the value is the hole current Ic. It multiplies by the unbalance resistance Rho. Hall voltage Vh Since it is minute, it is inputted and amplified by the differential amplifying circuit 102 of an amplification factor G. A common mode voltage Vcm is removed by this differential amplifying circuit 102. Although the output of a differential amplifying circuit 102 is inputted into an integrating circuit 103 and it integrates with it, offset voltage Rho is removed for every period of offset voltage at this time. Therefore, electrical-potential-difference value GxVh which is equivalent to electric energy in an integrating circuit 103 It is detected.
[0003]
[Problem(s) to be Solved by the Invention] In the case of the circuitry of drawing 3 , a common mode voltage Vcm is removed by using a differential amplifying circuit, but the input offset voltage of the operational amplifier which constitutes a differential amplifying circuit, and the offset voltage by input bias current occur as an error factor. The value of the Hall voltage in a light load is microvolt order, and even if it uses a highly precise operational amplifier, these offset voltage values serve as this level, and cause gross errors.
[0004] Drawing 4 is two operational amplifiers OP1 about a differential amplifying circuit, in order to solve such a trouble. OP2 It is the basic configuration of the constituted circuit. Operational amplifier OP1 OP2 They are input offset voltage Vio1 and Vio2, respectively. And it has input bias current Ib1 and Ib2. By this circuitry, the output of a differential amplifying circuit 102 is set to -(1+R2/R1) (-Vh-Vho+Vio1-Vio2)-R2 (Ib1-Ib2), and is input offset voltage Vio1 and Vio2. The offset voltage by input bias current Ib1 and Ib2 is overlapped. However, R1 and R2 It is resistance. However, operational amplifier OP1 OP2 As for the offset voltage to depend, forward negative polarity appears reversely respectively. For this reason, it is made on the same pellet, and if the operational amplifier which guaranteed the tracking property is used, it will be set to Vio1 **Vio2 and Ib1**Ib2, and offset voltage will be negated. However, although it is the operational amplifier which guaranteed the tracking property, neither input offset voltage nor input bias current necessarily becomes completely equivalent, and it may become an error factor in case highly precise measurement is carried out in a light load. Moreover, when using the operational amplifier which has not guaranteed the tracking property, the circuit of drawing 4 cannot remove an error.
[0005] As a cure to these troubles, a hole current is reversed periodically, the reversal is returned in the latter

part of a differential amplifying circuit, and there is a method of removing the offset voltage generated in the meantime in an integrating circuit. Drawing 5 is drawing showing the basic configuration of such a circuit. SWa1, SWa2, SWb1, and SWb2 are change-over switches, and SWa1 and SWa2 are ON between the reversal periods a, and between OFF and the reversal period b, SWb1 and SWb2 are controlled by the signal from a non-illustrated reversal clock circuit by the reverse, and they change the sense of a hole current with it. The output of the hall device between the reversal period a and the reversal period b serves as a:-Vh-Vhob:Vh+Vho, and the output of the differential amplifying circuit 102 after removing a common mode voltage Vcm is set to a:G1(-Vh-Vho+Vio1-Vio2)-R2 (Ib1-Ib2) b:G1(Vh+Vho+Vio1-Vio2)-R2 (Ib1-Ib2). G1 It is the gain of a differential amplifying circuit 102, and is - (1+R2 / R1). Here, between the reversal periods b reverses the output of a differential amplifying circuit 102 by the inverting circuit 104. That is, the output of an inverting circuit 104 is set to a:G1(-Vh-Vho+Vio1-Vio2)-R2 (Ib1-Ib2) b:G1(-Vh-Vho-Vio1+Vio2)+R2 (Ib1-Ib2). When these both are compared, since the polarity of return and an offset component is carrying out the positive/negative inversion at the polarity with the same Hall voltage, it is input offset voltage Vio1. Even if Vio2 and input bias current Ib1 and Ib2 are not equal respectively, it becomes removable [offset voltage] with the period which doubled the reversal periods a and b by the integrating circuit 103. Therefore, if electric energy is detected when the period of offset voltage and the period of a reversal clock synchronize, the error factor of both offset voltage and offset voltage is removable. Therefore, dividing of the zero cross signal of the measurement electrical potential difference V will be carried out, and the reversal clock signal which synchronized with offset voltage will be made. However, since it was difficult for the precision of the measurement electrical potential difference V which becomes origin to make a reversal clock signal with duty ratio a:b equal to 1:1 from the condition of having synchronized with offset voltage well, also in the circuit of drawing 5 , offset voltage might remain without being removed thoroughly and might cause an error.

[0006] (The object of invention) The object of this invention is offering the watthour meter using the hall device which can remove the offset voltage of the hall device leading to an error, and the offset voltage of a differential amplifier means with high degree of accuracy.

[0007]

[Means for Solving the Problem] In order to attain the above-mentioned object, this invention outputs the Hall voltage which is equivalent to the product of a measurement electrical potential difference and a measurement current with a hall device. The polarity of the positive/negative of said Hall voltage is reversed for every predetermined period with a switching means. Carry out a differential amplifier with a differential amplifier means, and the condition that polarity reversals according the polarity of the differential amplifier output of said differential amplifier means to said switching means returned with the reversal means is re-reversed. In the watthour meter using a hall device with which it integrated with the integral means Two hall devices which output different polar offset voltage from the same polar Hall voltage as said hall device are used. It adjusts so that the offset voltage of said two hall devices may become equal with an unbalance voltage adjustment means, and it is characterized by adding each differential amplifier output of said two hall devices with an addition means before the integral by said integral means.

[0008]

[Embodiment of the Invention] Drawing 1 is drawing showing the basic configuration of the watthour meter using the hall device which is one gestalt of operation of this invention. 1 and 2 are hall devices, and they arrange a front flesh side to the reverse sense to the field B equivalent to a measurement current so that the sense of a field may hit reversely respectively. The same hole current Ic which is furthermore equivalent to the measurement electrical potential difference V by the hall device 1 and the hall device 2 The forward negative polarity of an input terminal is reversely connected so that it may flow to the reverse sense. SWa1, SWa2, SWb1, and SWb2 are change-over switches, SWa1 and SWa2 are ON between the reversal periods a, and SWb1 and SWb2 are controlled by the signal (it is not necessary to synchronize with offset voltage Vho1 and Vho2) of the duty ratio 1:1 from a non-illustrated reversal clock circuit by the reverse between OFF and the reversal period b. Hole current Ic inputted into hall devices 1 and 2 by this The sense is periodically reversed. The differential amplifying circuits 3 and 4 for removing a common mode voltage, respectively and the delta sigma circuits 5 and 6 which perform A/D conversion are connected to the output side of hall devices 1 and 2.

[0009] Hall voltage Vh1 and offset voltage Vho1 which are generated between the output terminals of a hall device 1 in the state of the reversal period a Since the forward negative polarity of an input terminal is connected reversely, it is set to Vh1=K1xBx(-Ic) Vho1=(-Ic) xRho1, and both become the value of minus.

Product sensitivity K1 And unbalance resistance Rho1 It is the constant which a hall device 1 has. Moreover, Hall voltage Vh2 and offset voltage Vho2 which are generated between the output terminals of a hall device 2 At the reverse sense, a front flesh side hits hard flow and Field B is [a hall device 1] the hole current Ic further. Set to Vh2=K2x (- B) xIcVho2=Ic xRho2 in order to flow to the reverse sense, Hall voltage Vh2 is minus and offset voltage Vho2. It is added. The polar offset voltage in which it differs from the same polar Hall voltage from between the output terminals of both the hall devices 1 and 2 similarly in the reversal period b is obtained.
[0010] It is inputted into a differential amplifying circuit 3, and the output of a hall device 1 is a common mode voltage Vcm1. Although removed, it is the operational amplifier OP1 in a differential amplifying circuit 3 in that case. And OP2 Input offset voltage Vio1 and Vio2 And offset voltage is overlapped on an output according to input bias current Ib1 and Ib2. Therefore, the output between the reversal period a of a differential amplifying circuit 3 and the reversal period b is set to a:G1(-Vh1-Vho1+Vio1-Vio2)-R2 (Ib1-Ib2) b:G1(Vh1+Vho1+Vio1-Vio2)-R2 (Ib1-Ib2). However, R1 and R2 Resistance and G1 It is the gain of a differential amplifying circuit 3, and is - (1+R2 / R1). The output of the differential amplifying circuit 4 similarly connected to the hall device 2 Operational amplifier OP4 in a differential amplifying circuit 4 And OP5 Input offset voltage Vio4 and Vio5 And if it is input bias current Ib4 and Ib5 It is set to a:G1(-Vh2+Vho2+Vio4-Vio5)-R2 (Ib4-Ib5) b:G1(Vh2-Vho2+Vio4-Vio5)-R2 (Ib4-Ib5). Because of simplification here of a formula, they are an operational amplifier OP1, OP2, OP4, and OP5. They are Vos1, Vos2, Vos4, and Vos5 about an offset component, respectively. It collects by carrying out. Namely, if Vos1=G1 xVio1-R2 xIb1Vos2=-G1xVio2+R2 xIb2Vos4=G1 xVio4-R2 xIb4 Vos5=-G1xVio5+R2 xIb5 The output of a differential amplifying circuit 3 to a:G1(-Vh1-Vho1) +Vos1+Vos2b:G1(Vh1+Vho1)+Vos1+Vos2 Moreover, the output of a differential amplifying circuit 4 is rewritten with a:G1(-Vh2+Vho2)+Vos4+Vos5 b:G1(Vh2-Vho2)+Vos4+Vos5.
[0011] The output of differential amplifying circuits 3 and 4 is the operational amplifier OP3 in the delta sigma circuit 5, and the operational amplifier OP6 in the delta sigma circuit 6 in that case, although A/D conversion is inputted and carried out to the delta sigma circuits 5 and 6, respectively. Input offset voltage Vio3 and Vio6 And it is further superimposed on the offset voltage by input bias current Ib3 and Ib6. They are Vos3 and Vos6 similarly about these offset components. If it carries out The output of the delta sigma circuit 5 serves as a:G1(-Vh1-Vho1)+Vos1+Vos2+Vos3 b:G1(Vh1+Vho1)+Vos1+Vos2+Vos3. The output of the delta sigma circuit 6 serves as a:G1(-Vh2+Vho2)+Vos4+Vos5+Vos6 b:G1(Vh2-Vho2)+Vos4+Vos5+Vos6. When the output of the delta sigma circuits 5 and 6 is measured as mentioned above, Hall voltage Vh1 and Vh2 is offset voltage Vho1 and Vho2 to being the same polarity. It is a reverse polarity. Therefore, offset voltage is removable by adding both. however, the offset voltage Vho1 of hall devices 1 and 2 and Vho2 **** -- since there is dispersion, the gain equalization circuit 7 is established in the latter part of the delta sigma circuit 6, and the output by the side of a hall device 2 is adjusted. The gain G2 of the gain equalization circuit 7 is addition result Vho1-G2 xVho2 of the output by the side of a hall device 1, and the output after the gain control by the side of a hall device 2, when only offset voltage is outputted between output terminals in the state of no-load [which does not give a field before measurement]. It adjusts so that it may be set to 0. namely, G2 =Vho1 / Vho2 it is . Therefore, the output of the gain equalization circuit 7 becomes a:G2x{G1(-Vh2+Vho2)+Vos4+Vos5+Vos6} b:G2x {G1 (Vh2-Vho2)+Vos4+Vos5+Vos6}. If this output and the output of the delta sigma circuit 5 are inputted and added to an adder circuit 8 Offset voltage Vho1 Vho2 It is denied. The output of an adder circuit 8 is set to a:-G1 xVh1+Vos1+Vos2+Vos3+G2 (-G1 xVh2+Vos4+Vos5+Vos6) b:G1xVh1+Vos1+Vos2+Vos3+G2 (G1xVh2+Vos4+Vos5+Vos6).
[0012] In order to return the Hall voltage reversed by reversal of a hole current here and to reverse the forward negative polarity of offset voltage, If between the reversal periods b reverses the output of an adder circuit 8 by the inverting circuit 9 The output of an inverting circuit 9 is set to a:-G1 xVh1+Vos1+Vos2+Vos3+G2(-G1 xVh2+Vos4+Vos5+Vos6) b:-G1 xVh1-Vos1-Vos2-Vos3+G2 (-G1 xVh2-Vos4-Vos5-Vos6). If these both are compared, Hall voltage Vh1 and Vh2 will serve as like-pole nature, and will serve as an altogether different polarity about offset voltage. Offset voltage will be removed, if the output of this inverting circuit 9 is inputted into the counting circuit 10 (it is equivalent to the integral means of an analog circuit) with a subtraction function and is integrated for every period of a reversal clock. That is, in the counting circuit 10 with a subtraction function, the Hall voltage value equivalent to -G1(Vh1+G2xVh2) = (1+R2/R1) (Vh1+G2 xVh2) and a power value is detected, and the electric-energy value according to it is integrated. In addition, the combination of a digital low pass filter and an updown counter is specifically as a counting circuit 10 with a subtraction function used. Moreover, other A/D converters can be used instead of the delta sigma circuits 5 and

6.

[0013] As explained above, according to the operation gestalt of drawing 1 , a circuit is constituted using two hall devices 1 and 2, and Hall voltage removes offset voltage because offset voltage adds the output of both the hall devices 1 and 2 used as antipole nature by like-pole nature. In order for the integral for every period not to remove offset voltage like the conventional technique, even when a measurement electrical potential difference carries out frequency change rapidly, offset voltage is removed with a sufficient precision. About offset voltage, like the conventional technique, after reversing a hole current periodically, it is returning reversal, and only the polarity of an offset voltage component is reversed periodically and it removes by integrating with it. Although the integral had removed two error factors, offset voltage and offset voltage, therefore the reversal clock needed to be synchronized with offset voltage with the conventional technique, offset voltage might be unable to be removed when the gap of duty ratio arose. According to the operation gestalt of drawing 1 , at the integral event, since offset voltage is already removed, it is not necessary to synchronize a reversal clock with offset voltage, and duty ratio can use an equal accurate crystal oscillator. Therefore, improvement in the clearance precision of an error factor can be aimed at. Furthermore, in order to connect two hall devices 1 and 2 to a serial, twice as many Hall voltage as this can be obtained without increasing a hole current, and it is strong in a noise and becomes the circuit which stopped the consumed electric current. In addition, although the example of drawing 1 was made into the example of a circuit for which analog processing and digital processing were intermingled, A/D conversion is not performed but the effectiveness same also in the circuit of only analog processing is acquired.

[0014] Drawing 2 is drawing showing other gestalten of operation of this invention. Although the delta sigma circuit 5 and the gain equalization circuit 7 of the 6 latter part are adjusting dispersion in the offset voltage of two hall devices 1 and 2 in digital one with the operation gestalt of above-mentioned drawing 1 , the operation gestalt of drawing 2 is an example which performs the adjustment according to a hole current. Hall devices 1 and 2 are connected to juxtaposition, and the hole current Ic1 flows to a hall device 1. Moreover, the hole current Ic2 flows to a hall device 2. When only offset voltage is outputted from between the output terminals of hall devices 1 and 2 as initial setting in the state of no-load [which does not give a field], it is addition result Vho1-Vho2 of the output by the side of a hall device 1, and the output by the side of a hall device 2. Variable resistance VR adjusts the hole current Ic2 so that it may be set to 0.

[0015] The sense of the hole current Ic1 inputted into a hall device 1 is controlled by change-over switches SWa1, SWa2, SWb1, and SWb2. Moreover, the sense of the hole current Ic2 inputted into a hall device 2 is controlled by change-over switches SWa3, SWa4, SWb3, and SWb4. It is SWa 1-4 between the reversal periods a. It is SWb 1-4 by ON. It is controlled by the reverse between OFF and the reversal period b, and the sense of the hole current inputted into hall devices 1 and 2 by this reverses it periodically.

[0016] Hall voltage Vh1 and offset voltage Vho1 which are generated between the output terminals of a hall device 1 in the state of the reversal period a Since the forward negative polarity of an input terminal is connected reversely, it is set to Vh1=K1xBx(- Ic1) Vho1=(-Ic) xRho1. Moreover, Hall voltage Vh2 and offset voltage Vho2 which are generated between the output terminals of a hall device 2 With the reverse sense, since the hole current Ic2 also flows [in / in a front flesh side / hard flow] to the reverse sense further, as for a hall device 1, Field B serves as Vh2=K2x (- B) xIc2Vho2=Ic2xRho2. The case of the reversal period b is same polar Hall voltage Vh1 and Vh2, different polar offset voltage Vho1, and -Vho2 from between the output terminals of both the hall devices 1 and 2 similarly. It is obtained.

[0017] It is inputted into a differential amplifying circuit 3, and the output of a hall device 1 is a common mode voltage Vcm1. Although removed, it is the operational amplifier OP1 in a differential amplifying circuit 3 in that case. And OP2 Input offset voltage Vio1 and Vio2 And offset voltage is overlapped on an output according to input bias current Ib1 and Ib2. Therefore, the output between the reversal period a of a differential amplifying circuit 3 and the reversal period b is set to a:G1(-Vh1-Vho1+Vio1-Vio2)-R2 (Ib1-Ib2) b:G1(Vh1+Vho1+Vio1-Vio2)-R2 (Ib1-Ib2). G1 It is the gain of a differential amplifying circuit 3, and is - (1+R2 / R1). The output of the differential amplifying circuit 4 similarly connected to the hall device 2 Operational amplifier OP3 in a differential amplifying circuit 4 And OP4 They are Vio3 and Vio4 about input offset voltage. And if input bias current is set to Ib3 and Ib4 It is set to a:G1(-Vh2+Vho2+Vio3-Vio4)-R2 (Ib3-Ib4) b:G1(Vh2-Vho2+Vio3-Vio4)-R2 (Ib3-Ib4). Because of simplification here of a formula, they are an operational amplifier OP1, OP2, OP3, and OP4. They are Vos1, Vos2, Vos3, and Vos4 about an offset component, respectively. It collects by carrying out. Namely, if Vos1=G1 xVio1-R2 xIb1Vos2=-G1xVio2+R2 xIb2Vos3=G1 xVio3-R2 xIb3Vos4=-

G1xVio4+R2 xIb4 The output of a differential amplifying circuit 3 to a:G1(-Vh1-Vho1)+Vos1+Vos2b:G1 (Vh1+Vho1)+Vos1+Vos2 Moreover, the output of a differential amplifying circuit 4 is rewritten with a:G1(-Vh2+Vho2)+Vos3+Vos4 b:G1(Vh2-Vho2)+Vos3+Vos4.

[0018] Although these both are added in an adder circuit 8, it sets to initial setting, and it is offset voltage Vho1. Vho2 Since it is adjusted so that it may become equal, after addition is negated. Therefore, the output of an adder circuit 8 serves as a:-G1 xVh1+Vos1+Vos2-G1xVh2+Vos3+Vos4 b:G1xVh1+Vos1+Vos2+G1xVh2+Vos3+Vos4, and the offset voltage which is an error component here is removed.

[0019] The output of an adder circuit 8 is the operational amplifier OP5 in the delta sigma circuit 5 in that case, although A/D conversion is inputted and carried out to the delta sigma circuit 5. It is further superimposed on input offset voltage Vio5 and the offset voltage by input bias current Ib5. It is Vos5 similarly about these offset components. If it carries out, the output of the delta sigma circuit 5 will serve as a:-G1 xVh1+Vos1+Vos2-G1xVh2+Vos3+Vos4+Vos5 b:G1xVh1+Vos1+Vos2+G1xVh2+Vos3+Vos4+Vos5. In order to return the Hall voltage reversed by reversal of a hole current here and to reverse the forward negative polarity of offset voltage, If between the reversal periods b reverses the output of the delta sigma circuit 5 by the inverting circuit 9 The output of an inverting circuit 9 serves as a:-G1 xVh1+Vos1+Vos2-G1xVh2+Vos3+Vos4+Vos5b:-G1 xVh1-Vos1-Vos2-G1xVh2-Vos3-Vos4-Vos5. If these both are compared, Hall voltage Vh1 and Vh2 will serve as like-pole nature, and will serve as an altogether different polarity about offset voltage. Offset voltage will be removed, if the output of this inverting circuit 9 is inputted into the counting circuit 10 with a subtraction function and is integrated for every period of a reversal clock. That is, in the counting circuit 10 with a subtraction function, the Hall voltage value equivalent to -G1(Vh1+Vh2) = (1+R2/R1) (Vh1+Vh2) and a power value is detected, and the electric-energy value according to it is integrated.

[0020] Thus, also in the operation gestalt of drawing 2 , improvement in the clearance precision of an error factor can be aimed at like the operation gestalt of drawing 1 . However, in the operation gestalt of drawing 2 , since two hall devices are connected to juxtaposition, in order to obtain the same Hall voltage as the operation gestalt of drawing 1 , a twice as many hole current as this is needed.

[0021]

[Effect of the Invention] Since according to this invention an addition means removes offset voltage and the integral means removed offset voltage as explained above, it can carry out to high degree of accuracy by being able to remove offset voltage with a sufficient precision, and removing offset voltage independently with clearance of offset voltage.

[Translation done.]

除去を不平衡電圧の除去と別々に行うことにより高精度に行うことができる。

【図面の簡単な説明】

【図１】本発明の実施の一形態である．ホール素子を用いた電力量計を示すブロック図である。

【図２】本発明の実施の他の形態である、ホール素子を用いた電力量計を示すブロック図である。

【図３】従来のホール素子を用いた電力量計の回路例を示すブロック図である。

【図４】従来のホール素子を用いた電力量計の別の回路例を示すブロック図である。

【図５】従来のホール素子を用いた電力量計の別の回路例を示すブロック図である。

＊【符号の説明】

１．２　ホール素子

３．４　差動増幅回路

５．６　デルタ・シグマ回路

７　利得調整回路

８　加算回路

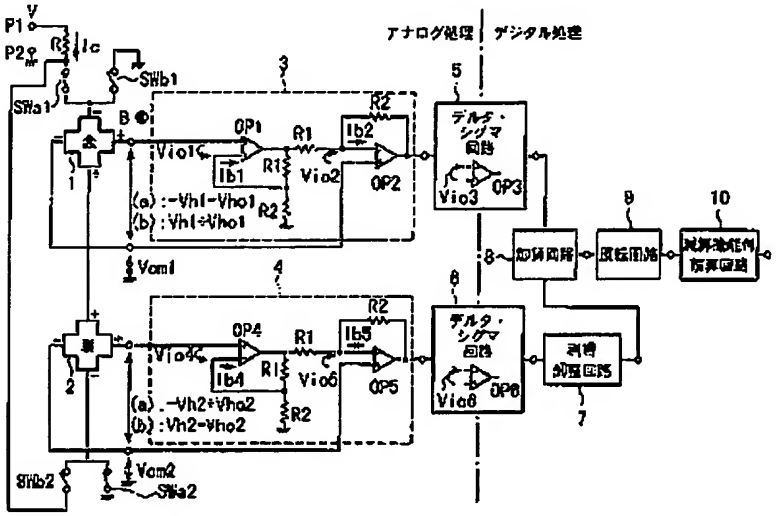
９　反転回路

１０　減算機能付積算回路

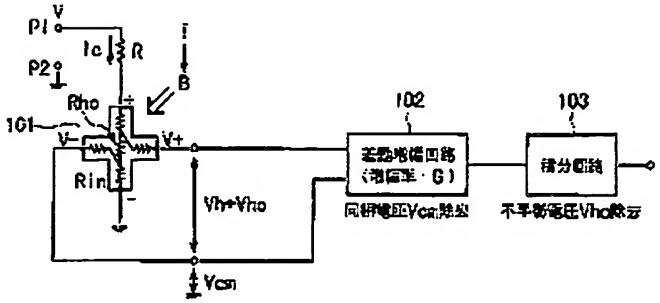
SWa1, SWa2, SWa3, SWa4, SWb1, SWb2, SWb3, SWb4　切換スイッチ

VR　可変抵抗

【図１】



【図３】



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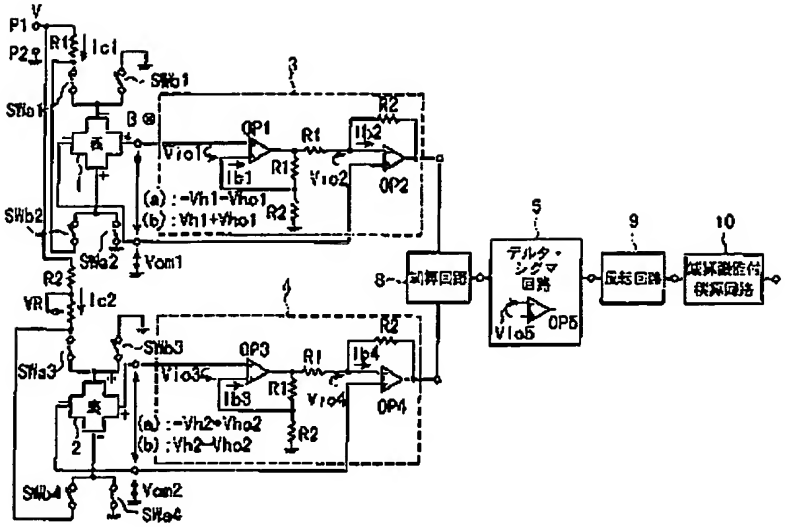
P1
P2
R1
Ic1
SWb1
SWa1
SWb2
SWa2
Vom1
R2
VR
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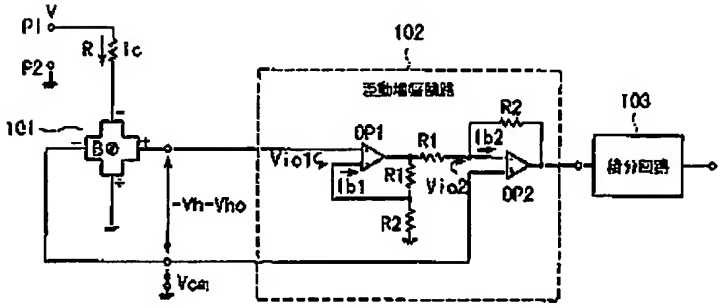
SWb4
SWa4
Vom2
OP1
OP2
OP3
OP4
OP5
Vio1
Vio2
Vio3
Vio4
Vio5
Ib1
Ib2
Ib3
Ib4
(a) :-Vh1-Vho1
(b) :Vh1+Vho1
(a) :-Vh2+Vho2
(b) :Vh2-Vho2
3
4
5
8
9
10
演算回路
デルタ・シグマ回路
反転回路

【図4】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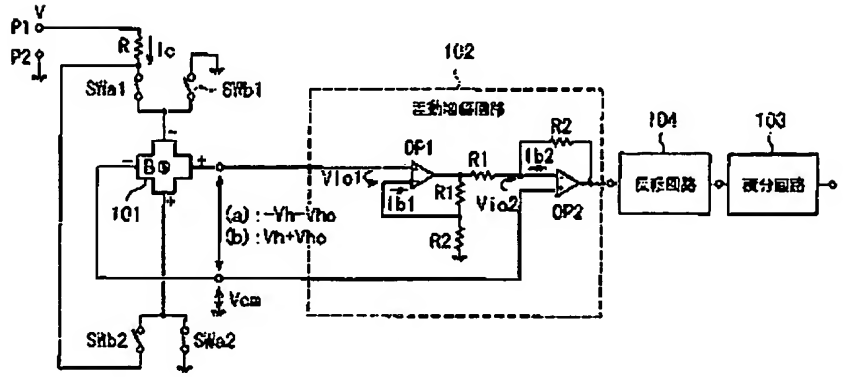
P2
R
Ic
101
102
103
R2
OP1
OP2
R1
Ib1
Ib2
Vio1
Vio2
-Vh-Vho
Vcm
積分回路

【図5】


P1
P2
R
Ic
SWa1
SWb1
101
102
103
104
R2
OP1
OP2
R1
Ib1
Ib2
Vio1
Vio2
(a) :-Vh-Vho
(b) :Vh+Vho
Vcm
SWb2
SWa2
反転回路
積分回路